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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,228	11/12/2003	Amir Hekmatpour	RPS920030129US1 (IRA-10-5	6310

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DRIGGS, LUCAS, BRUBAKER & HOGG CO. L.P.A.
38500 CHARDON ROAD
DEPT. IRA
WILLOUGBY HILLS, OH 44094

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,228	HEKMATPOUR, AMIR	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,7,9,10 and 13-20* is/are rejected.

7)☒ Claim(s) *3,4,6,8,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/706,228 filed on 11/12/2003. Claims 1-20 remain pending in the application.

Claim Objections

2. Claims 1, 4, 5, 6, 8, 9, 12, 18 and 20 are objected to because of the following informalities: in step b), "the simulated behavior of design models" lack antecedent basis; in step c), "the traces of the simulation generated by the verification process" lack antecedent basis; in step d), "the simulation database" should be changed to –the simulation traces database--; in step e), "the test generators and engineers" should be changed to –the test generator and verification engineers--; in step f), "the test program database" should be changed to –the test programs database--; in step g), "all functional coverage analysis data and coverage model results" needed clarification in reference to Fig. 2 and specification; in step h), "the coverage models" needed clarification in reference to Fig. 2 and specification; in step l), "a coverage analysis program" needed clarification in reference to Fig. 2 and specification; in step m), "the created coverage models" should be changed to –the created architectural coverage models--. In addition, applicant is requested to indicate each of the claimed limitations in reference to Fig. 2 and specification in order to clarify the specific claimed limitations which applicant intends to refer to. (Note that, for examination purpose, a program as recited in the claim is the same one). Claim 4, "the capability of providing" should be changed to –providing--, in order to provide concise claimed language. Claim 5, "the coverage analysis" should be changed to –the coverage analysis program--. Claim 6,

"the coverage analysis environment" lacks antecedent basis and needed clarification in reference to Fig. 2 and specification. Claim 8, "using these as input", needed to be more specific. Claim 9, in step b), "the design models" should be changed to –simulated behavior of design models--; in step c) "the test program database" should be changed to –the test programs database--; in step d), "storing the models" should be changed to –storing the created architectural and microarchitectural coverage models--. Claim 9, "the optimized test specs" lacks antecedent basis. Claim 12, "these tests" needed to be more specific (suggest: the deterministic tests). Claim 18 is also objected for similar reasons as in the objection of claim 1. Claim 20, "may be used' needed to change to be more concise claimed language (suggest: being used). Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 6,647,513. As to claims 1-8 and 18-20, although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claims refer to a method/system for verification including a coverage analysis of functional verification of integrated circuit designs suggest all claimed limitations except a program for mining and analyzing. It would have been obvious to one of ordinary skill in the art that the patent claims would suggest a program for mining and analyzing the databases in order to monitor the functional coverage and optimize the functional coverage database by adding the second test description's corresponding coverage attributes to the functional coverage database is the coverage achieved the second test description satisfies the test specification. As to claims 9-15, although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claims refer to a method/system for verification including a coverage analysis of functional verification of integrated circuit designs suggest all claimed limitations except mining and analyzing and creating/storing microarchitectural coverage models. It would have been obvious to one of ordinary skill in the art that the patent claims would suggest mining and analyzing the databases in order to monitor the functional coverage and optimize the functional coverage database by adding the second test description's corresponding coverage attributes to the functional coverage database is the coverage achieved the second test description satisfies the test specification; and the additional test description's corresponding coverage attributes to the functional coverage database

would suggest creating/storing microarchitectural coverage models in order to update the coverage models.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2, 5, 7 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawabe et al. (US 2004/0006751 A1).

7. As to claims 1 and 18, Kawabe et al. teach substantially similar claimed limitations of a method system for a providing a coverage analysis of functional verification of integrated circuit designs (Fig. comprising a) a test generator (test program); b) a simulator (functional simulator, instruction set simulator); c) a database containing simulation traces (functional verification result database, simulation result database); d) a program for mining and analyzing the simulation traces database (coverage checker, functional checker); e) a database of all test programs generated by the test generator and engineers (functional verification result database, simulation result database); f) a program for mining and analyzing the test program database (coverage checker, functional checker); g) a database of all functional coverage analysis data and coverage model results (coverage database, annotation database,

verification result); h) a program for mining and analyzing the functional coverage database (coverage checker, functional checker); i) a program for mining and monitoring of the coverage models (coverage checker, functional checker); j) a program for automatic test spec generation from design HDL (HDL, test programs); k) a program for test adjustment and optimization (coverage checker, verification item, annotation database, event database, coverage database); l) a coverage analysis program for creating architectural coverage models of the test programs (coverage database, coverage checker, annotation database); and m) functional coverage database for storage of the created coverage models (coverage database) (Fig. 1).

8. As to claims 2, 5 and 7, Kawabe et al. teach generating test program from HDL (Fig. 1); coverage checker detects verification trends and patterns and to report the same (Fig. 1); HDL of the design specification (Fig. 1).

9. As to claim 19, Kawabe et al. teach a coverage database for functional description of an LSI to be designed and modified (Fig. 1).

10. As to claim 20, Kawabe et al. teach a generated coverage database is used based on the analysis of the test programs database, and simulation traces database, and the mining of the said databases (Fig. 1).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 9-10 and 13-17 are rejected under 35 U.S.C. 103(a) as being obvious over Kawabe et al. (US 2004/0006751 A1).

13. As to claim 9, remarks set forth in rejecting claim 1 equally apply except for generating microarchitectural coverage models. Kawabe et al. teach verifying target architecture within the system LSI (LSI comprising a microprocessor, a memory or the like). Kawabe et al. suggest the results of simulation can be used to automatically and reliability check whether or not a verification item set by a designer has been actually tested. This enables a reliable check as to which verification item has been verified, and enables a reduction in costs required to create a test program for verification (0049). It is possible to easily detect a test program that has become unfocused activity or must be modified as a result of a change in functional description of an LSI to be designed (0050). These suggestions would have been obvious to practitioners in the art that in order to verify microarchitectural models, microarchitectural coverage models would have created and stored in the functional coverage analysis environment (coverage database).

14. As to claims 10, Kawabe et al. teach test program can be modified according to modified functional description of LSI design (0050).

15. As to claim 13, remarks set forth in rejecting claim 5 equally apply because of similar claimed limitation.

16. As to claim 14, Kawabe et al. teach automatically and manually generating event information and stored in annotation database (0042-0043). The simulation results

carried out a test program are with event information and are used to verify whether or not a verification item set by a designer has been actually tested. Thus it is possible to easily detect a test program that has become unfocused activity or must be modified as a result of a change in functional description of an LSI to be designed.

17. As to claims 15-17, Kawabe et al. teach a coverage database for functional description of an LSI to be designed and modified (Fig. 1).

Allowable Subject Matter

18. Claims 3, 4, 6, 8 and 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims; and if rewritten to overcome the claim objections as above suggestion. The prior art of record does not teach fairly suggest the feedback steps as recited in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER